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Traditional 6T-SRAM Performance Evaluation using Leakage-Power Reduction Techniques

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ABSTRACT— This technology uses a single-bit SRAM cell with an amplification circuit for current and charge sensing. Two further power-saving strategies are the footer stack and MTCMOS. Single-bit SRAM cells based on charge transfer sensing amplifiers perform unexpectedly well in terms of power efficiency and data retrieval times. The average power dissipation of the current sensing amplifier was reduced by 1 to 5 percent when employing the footer stack technique as opposed to MTCMOS. This approach mimics an array structure because it may be scaled to any number of dimensions without experiencing performance degradation.

Keywords — Static random access memory (SRAM), current mode sense amplifier (CMSA), Pre-charge Circuit (PCH), Charge-Transfer sense amplifier (CTSA), Multi threshold complementray metal oxide semiconductor (MTCMOS).

1. Introduction

Recently, there has been a lot of interest in using high-speed SRAM as a cache memory in mobile devices and data processing [1]. Nevertheless, despite advancements in submicron technology and component miniaturization, the number of devices on a chip is rising. This scaling technique suffers from stability and power loss weaknesses [2]. The sensing amplifier is a crucial circuit component that retrieves data from the selected memory [3]. The effectiveness of memory operation affects both power consumption and access times. Voltage, current, and charge transfer are the main constituents of amplifier circuits. Capacitances on the bit lines can slow down the voltage mode detecting amplifier frequently found in memories [4]. As a result, data processing times will be much enhanced. Current mode sensing amplifiers are much faster than their voltage-mode counterparts because they measure the current in the cell rather than the voltage [5].

The charge-transfer sense amplifier is one of several effective and useful ways to reduce power usage. Comparatively speaking to a traditional voltage mode sensing amplifier, the bit line swing and, thus, the bitline energy are minimized. To reduce latency and power consumption, we used cadence virtuosity to develop a single-bit SRAM cell that includes current sensing and charge transfer sense amplifiers [6]. Memory arrays frequently have large sizes. High-end embedded SRAMs only take up around half of the chip area, compared to standalone SRAMs, which can take up to 70% of the chip area. Researchers have designed and built a precharge circuit, a write driver circuit, and an SRAM. This group of sensory amplifiers was created and installed with a uniform width [7].

2. Low Leakage Power Reduction Methods

The section describes the operation of some of the basic techniques for reducing leakage power, such as MTCMOS and footer stack, to quantify the power loss and delay in sense amplifier circuits.

2.1 MTCMOS

This technique has eight potential implementations, all of which are dynamically adaptable. Vt values on the non-critical path are set high, while Vt values on the critical path are set low to reduce leakage power. In the dynamic approach, the Vt value of functional blocks connected to the virtual GND line is decreased. The on/off state is determined by high Vt, which wants GND [9].

2.2 Footer-Stack Technique:

The use of an MTCMOS version is one alternate strategy. In MTCMOS, the pull-up n/w and VDD are coupled using a P MOS, whereas the pull-down n/w and GND are coupled using an N MOS. In this configuration, two broader than usual transistors are stacked on top of one High Vt transistor. Leakage power can be decreased by placing numerous non-inverting transistors along the path [10].

3. SRAM Architecture

3.1 Conventional SRAM

Static random-access memory, or SRAM, keeps data safe even when the device is turned off. The data in an inverter controls the output of a single-bit static random-access memory (SRAM) cell [11]. Two stable states, two inverters, and two access transistors make up each cell's four parts. A memory cell can only hold the logical values 1 and 0, the only two conceivable values. The bit lines of an SRAM cell allow data to be read from and written to it, as depicted in Figure 1. The most common type of memory cell is standard random-access memory (SRAM) since it is dependable and uses very little power when not in use. The bit-line connected access transistors in the cell are turned on by setting WL to 1. Literacy is therefore feasible.

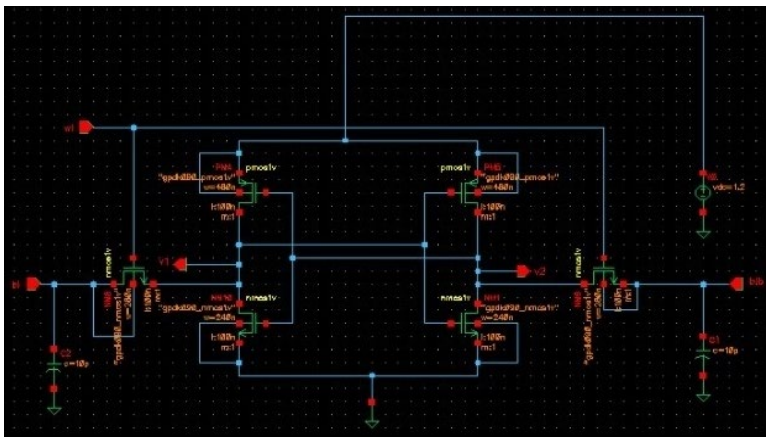

Figure1: A typical SRAM device is shown in this diagram.

3.2 Write Driver Circuit

The write-discharge circuit (WDC) [14] reduces the write margin of the SRAM cell in proportion to the peak PCH level by lowering the voltage on the bit lines. To commit data to a bit line, WDC will levy a fee. Figure 2 illustrates how the matching bit pin is written with the value of the bit lines when WE = 1. (i.e., when WE are enabled). The memory cell is programmed by the access transistor using the voltage read from the bit line.

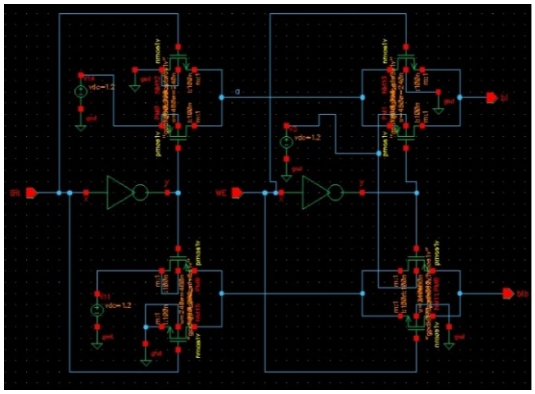

Figure2: diagram representation of a written driver circuit

3.3 Precharge Circuit

Before data can be read from or written to an SRAM, the bit lines must first be charged by a precharge circuit (PCH). In a PCH circuit, two complementary metal-oxide semiconductors (PMOS) transistors simultaneously produce a signal and the PCH clock. A third transistor is added between the bit lines to stop voltage swings while charging [15]. For a read operation to succeed, both bit lines must be at the same voltage. The voltage difference between the bit lines decreases once a read/write operation is finished. The PCH circuit subsequently raises the voltage of the bit lines until they are at the same level as the supply voltage, as depicted in Figure 3.

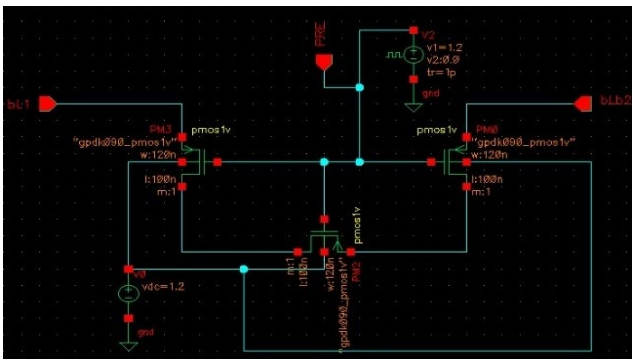

Figure3: depicts the precharge circuit's construction.

3.4 Sense Amplifier's

3.4.1 Current-Mode Sense Amplifier

Using CMSA functionalities requires monitoring the voltage on the data line. Voltage differences between bit lines are challenging to detect. The low-going bit line uses less power than a VMSA during the bit line precharge because it can be clamped at a higher voltage. Figure 4 shows a schematic illustration of the CMSA. It was created using [16] as a construction manual. The circuit's two parts are joined together. During the precharge phase, the nodes V3 and V4 are pre-discharged to GND to make room for the large current arriving from nodes V5 and V6. Current flows across nodes V3 and V4 at all times in the simulation while Ysel is connected to the ground because of the PMOS drain. The constant current in the cell cancels out any variations in the V3 and V4 currents. When the Saen is raised, two inverters stop the sensing amplifier from turning on. The flow of bias current through the bit lines of the sensing amplifier can modify the voltages of V5 and V6. The voltage is raised to CMOS logic levels using high-gain positive feedback and cross-coupled inverters.

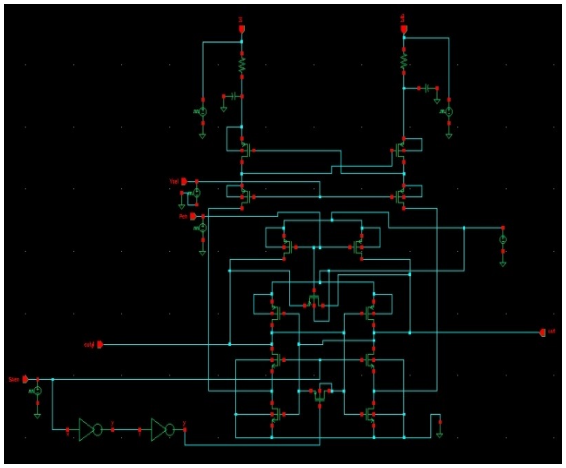

Figure4: CMSA configuration is shown.

3.4.2 Charge-Transfer Sense Amplifier

Using CMSA functionalities requires monitoring the voltage on the data line. Voltage differences between bit lines are challenging to detect. The low-going bit line uses less power than a VMSA during the bit line precharge because it can be clamped at a higher voltage. Figure 4 shows a schematic illustration of the CMSA. It was created using [16] as a construction manual. The circuit's two parts are joined together. During the precharge phase, the nodes V3 and V4 are pre-discharged to GND to make room for the large current arriving from nodes V5 and V6. Current flows across nodes V3 and V4 at all times in the simulation while Ysel is connected to the ground because of the PMOS drain. The constant current in the cell cancels out any variations in the V3 and V4 currents. When the Saen is raised, two inverters stop the sensing amplifier from turning on. The flow of bias current through the bit lines of the sensing amplifier can modify the voltages of V5 and V6. The voltage is raised to CMOS logic levels using high-gain positive feedback and cross-coupled inverters.

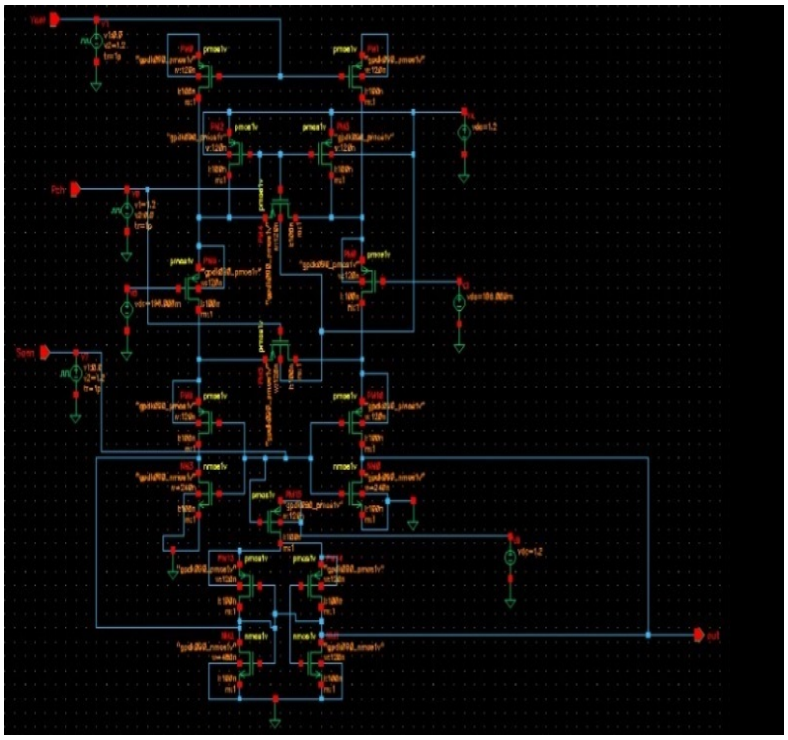

Figure 5: shows the inner workings of the CTSA.

4. Results and Discussion

The block design used to represent the architecture of a single-bit SRAM cell is shown in Figure 6 [18]. To make this design work, current-mode and charge-transfer-mode sensing amplifiers must be adjusted. A differential sensing amplifier, an SRAM cell, a hub for the program counter, and a word data converter are all components of the SRAM architecture.

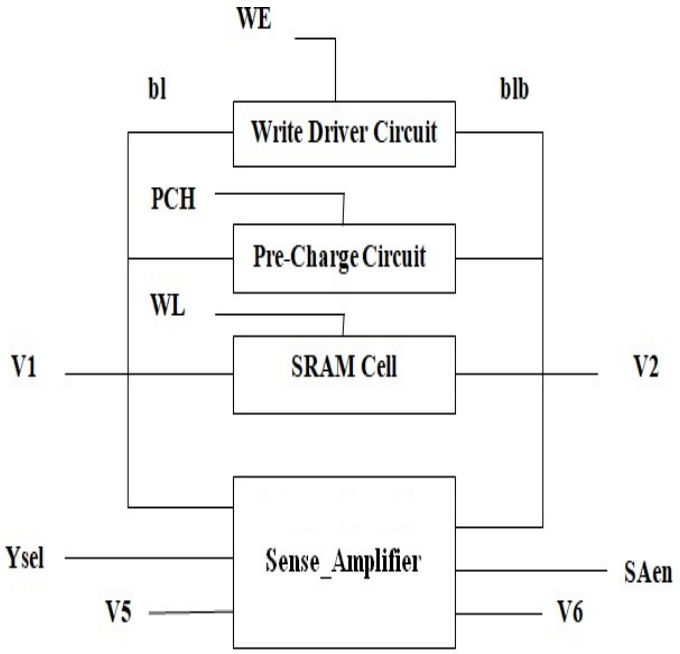

Figure 6: the components needed comprise a single-bit SRAM.

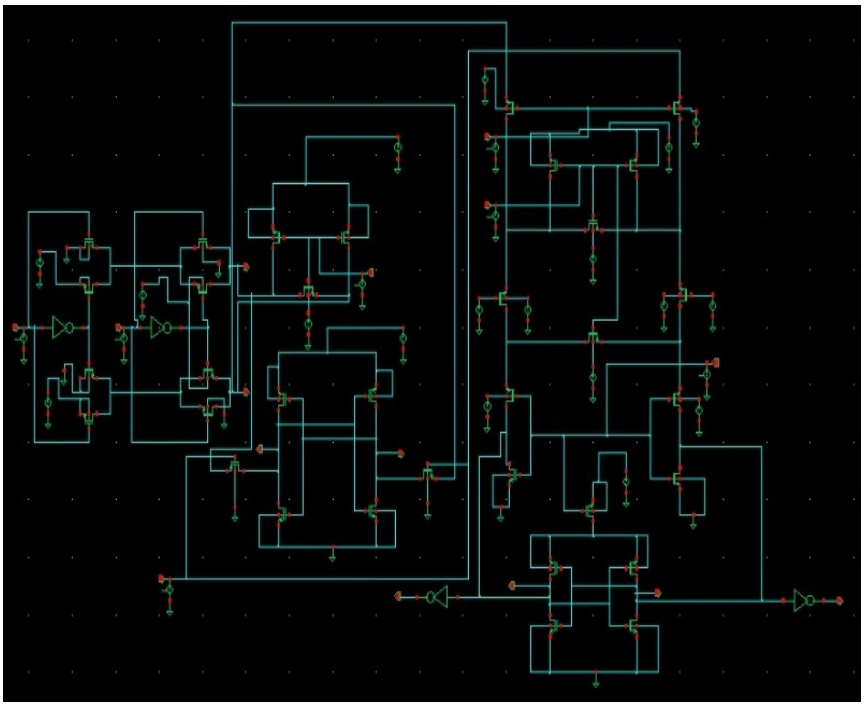

Figure 7: depicts a cell of an SRAM design with a PCH, WDC, and CTSA.

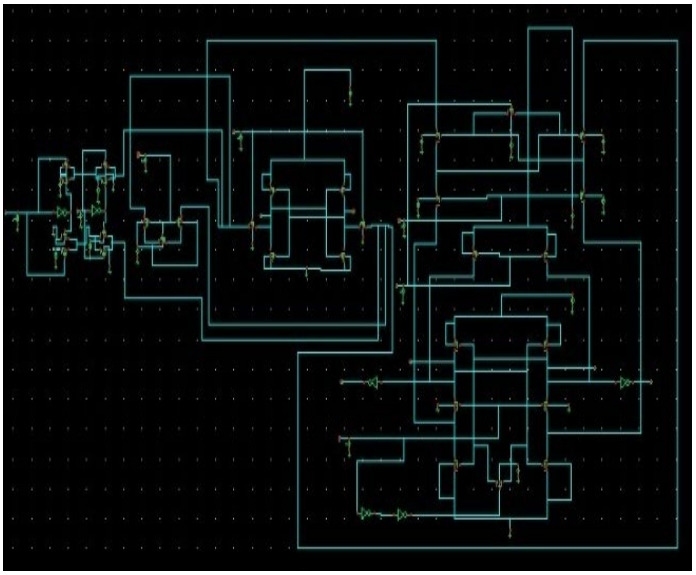

Figure 8: depicts a cell of an SRAM design with a PCH, WDC, and CMSA.

Figures 7 and 8 show block diagrams of how CTSA and CMSA are implemented in the SRAM design. WDC, bl, and blb each come to an end in the SRAM cell. When WL is set to 1, the results are stored in the memory cell instead of not being put there by default. The sensing amplifier in the reading operation is turned on when Saen is set to 1.

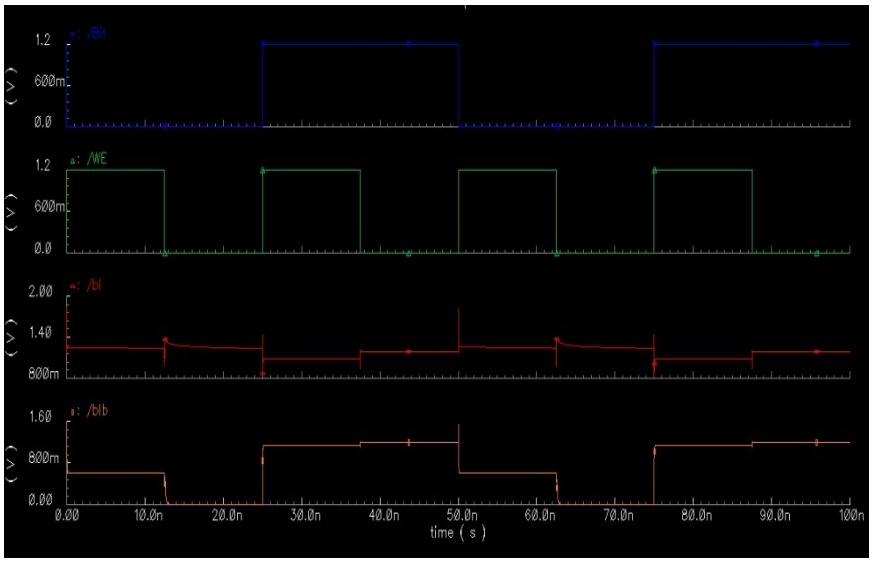

Figure 9: shows the output waveform of the WDC.

Figure 9 shows the waveform of the WDC output. When the WE is active, the bit is saved in bl and its complement in blb. The contents of a memory cell are copied in bl and blb when WE are turned off (WE = 0). Figures 10 and 11 show waveform samples for the CMSA and the CTSA, respectively. It is established that V5 = Bit i/p and V6 = Bit i/complement are the values of SAen = 1.

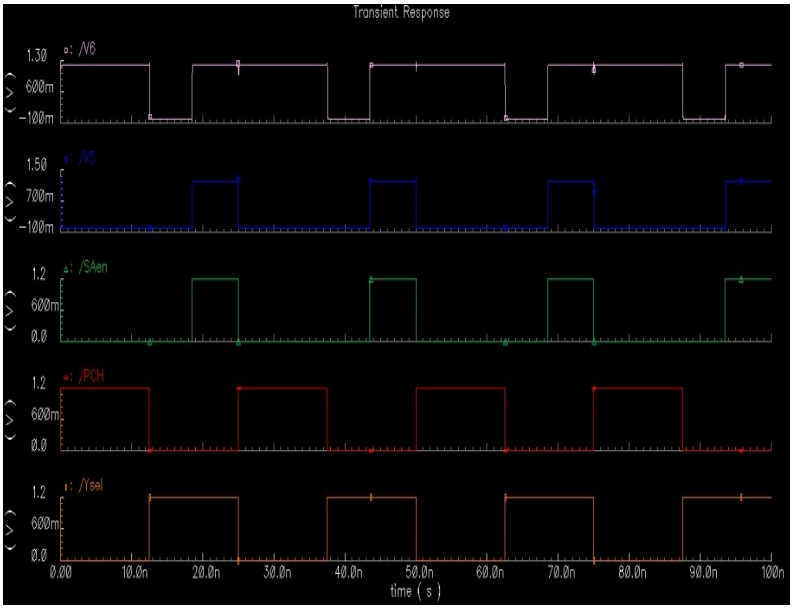

Figure10: The waveform of CMSA

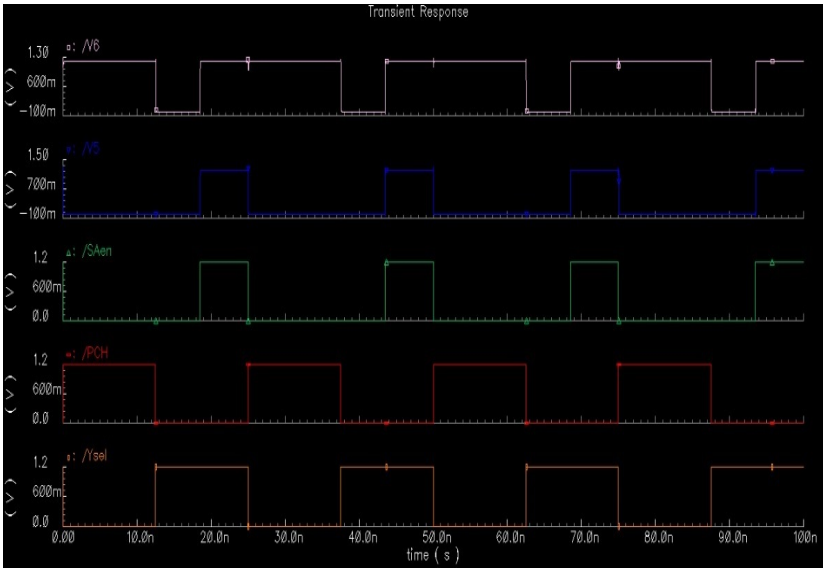

Figure11: The waveform of CTSA

Tables 1 and 2 show the energy usage for a single-bit SRAM cell architecture utilizing a modified CTSA and a CMSA, respectively. When MTCMOS techniques are combined with a single-bit SRAM cell architecture, it is possible to reduce the power consumption of the typical CMSA by 1 to 5 percent. MTCMOS, single-bit SRAM cells, and footer stack techniques can cut power consumption by 1%.

Table1. Cells in SRAM architectures using CMSA and CTSA typically consume power and delay

Parameters	SRAM with CMSA Architecture	SRAM with CTSA Architecture
Write Delay	22.34ηs	21.09ηs
Average Power Consumption	250.56μW	209.75μW

Read Delay	21.01ηs	20.58ηs

Table2. SRAM cell with modified CMSA and CTSA power consumption

Techniques Used	Using Modified CMSA to build Architecture	Using Modified CTSA to build Architecture
Footer-Stack Technique	270.89µW	213.58µW
MTCMOS Technique	275.89µW	214.85µW

5. Conclusion

The technique described here employs a current- and charge-sensing amplification circuit embedded within a single-bit SRAM cell architecture. Other methods for reducing power consumption have also been developed, such as MTCMOS and footer stack. Power efficiency and data retrieval times are areas where charge transfer sensing amplifier-based single-bit SRAM cells excel. In addition, the present sense amplifier's average power dissipation was reduced by 1-5% compared to MTCMOS, thanks to the footer stack technique. The work shown here can be scaled to any dimension without sacrificing performance, giving the impression of an array structure.

References

[1] Kobayashi, Masaharu, Nozomu Ueyama, and Toshiro Hiramoto. "A non-volatile SRAM integrated with a ferroelectric HfO2 capacitor for normally-off and ultralow power IoT application." In *VLSI Technology, 2017 Symposium on*, pp. T156-T157. IEEE, 2017.

[2] Pandey Sunil, Yadav Shivendra, Nigam Kaushal, Sharma Dheeraj, and Kondekar P. N. "Realization of Junction-less TFET-Based Power Efficient 6T SRAM Memory Cell for the Internet of Things Applications." In Proceedings of First International Conference on Smart System, Innovations and Computing, Springer, pp. 515-523. Springer, Singapore, 2018.

[3] Mohammad Baker, Dadabhoy Percy, Lin Ken, Bassett Paul. "Comparative study of current mode and voltage mode sense amplifier used for 28nm SRAM." 24th International Conference on Microelectronic, March 2013.

[4] Jeong, Hanwool, Oh Tae Woo, Song Seung Chul, and Jung Seong-Ook. "Sense-Amplifier-Based Flip-Flop with Transition Completion Detection for Low-Voltage Operation. The future issue of IEEE Transactions on Very Large-Scale Integration (VLSI) Systems (2018).

[5] Shalini, Kumar Anand "Design of high speed and low power sense amplifier for SRAM applications" International Journal of Scientific & Engineering Research, Volume 4, Issue 7, July-2013.

[6] Kiyoo Itoh, Masashi Horiguchi, and Hitoshi Tanaka "Ultra-Low Voltage Nano-Scale Memories," Springer 2007.

[7] Naik Sthrigdhara, Kuwelkar Sonia, "A Novel 8T SRAM with Minimized Power and Delay, "2nd IEEE International Conference on Recent Trends in Electronics Information & Communication Technology", PP.1498-1501, 2017, India

[8] Priya M. Geetha, Baskaran Dr.K., D. Krishnaveni. "Leakage Power Reduction Techniques in Deep Submicron Technologies for VLSI Applications." ELSEVIER, International Conference on Communication Technology and System Design, 2011, Procedia Engineering, 2012, 30, 1163 – 1170.

[9] Abdollahi Afshin, Fallah Farzan, Abdollahi Massoud, "A Robust Power Gating Structure and Power Mode Transition Strategy for MTCMOS Design," Very Large-Scale Integration (VLSI) Systems IEEE Transactions,2007. vol. 15, pp. 80-89.
[10] Panwar Shikha, Piske Mayuresh, Madgula Vivek Aatreya, "Performance Analysis of Modified Drain Gating Techniques for Low Power and High-Speed Arithmetic Circuits," Hindawi Publishing Corporation VLSI Design, Volume 2014, Article ID 380362, 5 pages.
[11] RAHMAN NAHID, SINGH B.P., "STATIC-NOISE-MARGIN ANALYSIS OF CONVENTIONAL 6T SRAM CELL AT 45NM TECHNOLOGY", INTERNATIONAL JOURNAL OF COMPUTER APPLICATION, MARCH-2013, VOLUME 66-NO.22.
[12] Tripathi Tripti, Chauhan D. S., Singh S. K., and Singh S. V. "Implementation of Low-Power 6T SRAM Cell Using MTCMOS Technique", In Advances in Computer and Computational Sciences, Springer, Singapore, 2017.
[13] Tiwari Nidhi, Gusain Srishti, Chakravorty Surabhi, Nirankari Ankita, and Khandelwal Apoorva. "Analysis and Optimization of Stability for 6T SRAM Cell Using 180 nm Technology." In Proceedings of the International Conference on Recent Cognizance in Wireless Communication & Image Processing, Springer, New Delhi, 2016.
[14] Gomes Iuri A.C., Meinhardt Cristina, Butzen Paulo F. "Design of 16nm SRAM Architecture" South Symposium on Microelectronics,2012.
[15] Bellerimath Preeti S, Banakar R.M., "Implementation of 16×16 SRAM Memory using 180nm technology," International Journal of Current engineering and technology, 2013.
[16] Sinha Manoj, Hsu Steven, Alvandpour Atila, Burleson Wayne, Krishnamurthy Ram, Borhr Shekhar. "High-Performance and Low-Voltage Sense-Amplifier Techniques for sub-90nm SRAM ." SOC Conference, Proceedings. IEEE International [Systems-on-Chip], 2003.
[17] Heller L. G., Spampinato D. P., Yao Y. L., "High-sensitivity charge-transfer sense amplifier," ISSCC Dig. Tech. Papers, 1975-Feb.
[18] Choudhary Richa, Padhy Srinivasa, Rout Nirmal Kumar, "Enhanced Robust Architecture of Single Bit SRAM Cell using Drowsy Cache and Super cut-off CMOS Concept," International Journal Of Industrial Electronics and Electrical Engineering, July 2015.